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(71) Applicant: 000006655
Nippon Steel Corporation
6-3 Ote-machi 2-chome
Chiyoda-ku, Tokyo-to
(71) Applicant: 000111096
Nittetsu Electron Corporation
11-12 Hatchobori 3-chome
Chiyoda-ku, Tokyo-to
(72) Inventor: Toshio IWASAKI
c/o Nippon Steel Corporation
6-3 Ote-machi 2-chome
Chiyoda-ku, Tokyo-to
(72) Inventor: Hirotsugu HAGA
c/o Nippon Steel Corporation
6-3 Ote-machi 2-chome
Chiyoda-ku, Tokyo-to
(72) Inventor: Masamichi OKUBO
c/o Nittetsu Electron Corporation
3434 Shimata-oaza
Hikari-shi, Yamaguchi-ken
(74) Agent: Mikio HATTA, Attorney

Specifications

(54) **[Title of the Invention]** Silicon Single Crystal and Manufacturing Method Thereof

(57) [Summary]
[Object] The objects of the present invention are to provide a silicon single crystal that has excellent device characteristics, as represented by post-device-heat-treatment oxide breakdown voltage, manufactured by the Czochralski method and a manufacturing method for such silicon single crystal.

[Composition of the Invention] In order to attain the above mentioned goals, manufacture of silicon single crystal by the Czochralski method according to the present invention is carried out such that the silicon single crystal cooling rate reaches a minimum within the temperature region of 850°C to 1200°C during manufacture. Preferably cooling rate within a T ± 100°C temperature region is less than or equal to 1.0°C/minute. Moreover, the silicon single crystal produced by the present invention has excellent oxide layer breakdown voltage characteristics such that oxide layer breakdown voltage A mode pass rate per wafer is less than 3%. [*TRANSLATOR'S NOTE: "Pass rate" looks like an error in the source text.*]

[Scope of the Patent Claims}

[Claim 1] A method for production of a silicon single crystal by the Czochralski method such that the silicon single crystal is cooled slowly through a certain temperature region during manufacture; wherein the temperature within this region at which cooling rate reaches a minimum is within the range of 1200°C to 850°C.

[Claim 2] A method for production of the silicon single crystal according to claim 1; wherein the cooling rate in the temperature region of T ± 100°C is less than or equal to 1.0°C/minute (T°C is the temperature for which cooling rate becomes a minimum within the slow cooling temperature region).

[Claim 3] A silicon single crystal manufactured by the method mentioned in claim 1 or claim 2; wherein after treatment of a silicon wafer sliced from the silicon single crystal by an additional 4-step heat treatment comprising treating for 110 minutes at 1000°C in a steam atmosphere; treating for 420 minutes at 1200°C in a nitrogen atmosphere; treating for 70 minutes at 900°C in a dry oxygen atmosphere; and treating for 130 minutes at 1000°C in a steam atmosphere; and after removal of the thermal oxide layer of a silicon wafer sliced from the silicon single crystal by dilute hydrofluoric acid solution, followed by formation upon the silicon wafer of numerous 25.0 nm insulation oxide layer thickness MOS diodes having 20 mm^2 surface area two-layer gate electrodes comprising an upper layer of aluminum and a lower layer of doped polysilicon; the silicon wafer then has excellent oxide layer breakdown characteristics such that evaluation of insulation oxide layer breakdown voltage characteristics of the wafer by the voltage ramping method, when applied to each MOS diode by application of DC polarity voltage to inject numerous carriers from the substrate silicon, results in a proportion of MOS diodes (relative to all of the MOS diodes) that is less then 3% showing a mean electrical field of 4.0 MV/cm or less when density of electrical current flowing through the oxide layer reaches 1 $\mu A/cm^2$.

[Detailed Explanation of the Invention]

[0001]

[Field of Industrial Use]

The present invention relates to a silicon single crystal and production method thereof by the Czochralski method (referred to hereinafter as the CZ method); wherein the silicon single crystal has excellent breakdown voltage characteristics of the oxide layer (referred to hereinafter as oxide layer breakdown characteristics).

[0002]

[Conventional Technology]

CZ silicon single crystal has conventionally been widely used as material for LSI since such single crystal is characterized as having excellent crystal strength. However, silicon single crystal oxide layer breakdown voltage is known to vary greatly according to fundamental differences in the production method. Oxide layer breakdown voltage of the single crystal wafer produced by the CZ method is markedly low in comparison to single crystal produced by the float zone method and single crystal produced by epitaxial growth upon CZ single crystal. However, in recent years in accompaniment with the increased degree of integration of MOS devices, there has been strong demand for improved reliability of the gate oxide layer, and development of a production method for CZ silicon single crystal that has an excellent oxide layer breakdown voltage characteristic, as one important indicator of reliability of the oxide layer, is seen as quite important.

[0003] A method for manufacture of a silicon single crystal of at least 100 mm diameter according to Published Unexamined Patent Application No. Hei 2-267195 produces CZ silicon single crystal that has excellent oxide layer breakdown voltage upon evaluation of wafers without additional heat treatment. This method in characterized in that crystal growth rate is 0.8 mm/minute or less. However, this method is unrealistic due to low productivity.

[0004] Moreover, Patent No. 174275 discloses a method for reduction of the density of oxygen precipitates during semiconductor device processing by performance of temperature control by slowly pulling the silicon single crystal for at least 3 hours through a temperature region as temperature falls from 1100°C to 900°C. However, no mention whatsoever is made of device characteristics as represented by oxide layer breakdown voltage characteristics.

[0005] Moreover, a manufacturing method for CZ silicon single crystal that has excellent oxide layer breakdown voltage upon evaluation of wafers without additional heat treatment is disclosed in Published Unexamined Patent Application No. Hei 5-70283. This proposes during manufacture of silicon single crystal a method of pulling such that the temperature region of 1150°C and higher of the growing silicon single crystal is at least 280 mm above the silicon melt (i.e., a method for gradual cooling in a temperature region limited to 1150°C and higher during pulling). However, as explained later, the inventors of the present invention discovered that the temperature region requiring gradual cooling in

order to improve oxide layer breakdown voltage characteristics is not the region of 1150°C and higher. Moreover, Unexamined Patent Application No. Hei 5-9096 has the goal of improving oxide layer breakdown voltage characteristics upon evaluation of wafers without additional heat treatment while suppressing generation of stacking faults. This publication proposes a method that utilizes a temperature control mechanism limited to use for decreasing the crystal cooling rate to limit crystal production rate to 0.8 mm/minute to 1.1 mm/minute. Each of these types of conventional oxide layer breakdown voltage improvement methods is limited to the case of wafers evaluated without additional heat treatment, uses slow cooling in a temperature region restricted to 1150°C and higher, or carries out crystal manufacture at a production rate limited by the use of a temperature control mechanism that has certain restrictions.

[0006] Therefore a method is needed for production of CZ silicon single crystal that has excellent oxide layer breakdown voltage; wherein the method doesn't cool slowly in a temperature region 1150°C and higher during the silicon single crystal production process, that doesn't restrict the slow cooling temperature region, and that doesn't restrict crystal production rate. Such a method hasn't previously existed. Moreover, although a method is needed for production of CZ silicon single crystal that has excellent oxide layer breakdown voltage characteristics upon evaluation of wafers after additional heat treatment similar to that of actual device processing, such a method hasn't previously existed.

[0007] Breakdown voltage characteristic of the insulation oxide layer is evaluated by forming MOS diodes over the entire surface of a silicon wafer; wherein the MOS diodes have 20 mm^2 surface area of two-layer gate electrodes comprising an upper aluminum layer and a lower doped polysilicon layer; wherein insulation oxide layer thickness is 25.0 nm. Evaluation is then performed by a voltage ramping method by application to each MOS diode of DC polarized voltage to inject numerous carriers from the silicon substrate. The region of mean electrical field below 4.0 MV/cm applied to the oxide layer when current density is 1 $\mu A/cm^2$ as current flows through the oxide layer is called the A mode region. This region indicates the presence of crystalline defects (referred to hereinafter as the cause of breakdown voltage degradation) that degrade oxide layer breakdown voltage characteristics within the crystal, or that the size of such crystalline defects is extremely large such that oxide layer breakdown voltage characteristics are markedly worsened. After a four-step additional heat treatment comprising: 110 minutes at 1000°C in a steam atmosphere, 420 minutes at 1200°C in a nitrogen atmosphere, 70 minutes at 900°C in a dry oxygen atmosphere, and 130 minutes at 1000°C in a steam atmosphere, followed by removal of the thermal oxide layer of a silicon wafer sliced from the silicon single crystal by dilute hydrofluoric acid solution so that the wafer undergoes additional heat treatment similar to that of actual device processing (referred to hereinafter as device heat treatment), the oxide layer breakdown voltage of conventional CZ silicon crystal (referred to hereinafter as the post-device-heat-treatment oxide layer breakdown voltage) is high as indicated by a ratio (proportion of MOS diodes having insulation breakdown in the A mode region relative to the total number of MOS diodes) of 5% to 15% per wafer. Therefore a CZ silicon single crystal that has a post-device-heat-treatment insulation breakdown of MOS diodes in the A mode region that is less than 3% of total MOS diodes is a CZ silicon crystal that has superior oxide layer breakdown voltage characteristics.

[0008]
[Problems to be Solved by the Invention] Therefore the objects of the present invention are to provide a method for the production of CZ silicon single crystal that has excellent device characteristics as represented by the post-device-heat-treatment oxide layer breakdown voltage characteristic and to provide a CZ silicon single crystal that has superior device characteristics as represented by the post-device-heat-treatment oxide layer breakdown voltage characteristic.

[0009]
[Means to Solve the Problems] In order to attain the above mentioned goals, the present invention is a method (present invention method (1)) for production of a silicon single crystal by the Czochralski method such that the silicon single crystal is cooled slowly through a certain temperature region during manufacture; wherein the temperature within this region at which cooling rate reaches a minimum is within the range of 1200°C to 850°C. Also in order to further improve post-device-heat-treatment oxide layer breakdown voltage characteristic, cooling rate in the temperature region of T ± 100°C is less than or equal to 1.0°C/minute (present invention method (2)).

[0010] After a silicon single crystal manufactured by the method of the present invention method (1) or (2) is sliced to form a wafer upon which additional device heat treatment is carried out, the wafer then has excellent oxide layer breakdown characteristics such that removal of the thermal oxide layer of a silicon wafer sliced from the silicon single crystal by dilute hydrofluoric acid solution, followed by formation upon the silicon wafer of numerous 25.0 nm insulation oxide layer thickness MOS diodes having 20 mm^2 surface area two-layer gate electrodes comprising an upper layer of aluminum and a lower layer of doped polysilicon, upon evaluation of insulation oxide layer breakdown voltage characteristics of the wafer by the voltage ramping method when applied to each MOS diode by application of DC polarity voltage to inject numerous carriers from the substrate silicon, results in an A mode rate per wafer that is less then 3%.

[0011]
[Operation of the Invention] The present invention will be explained below using figures and tables.

[0012] Figure 1 shows a cross section of a MOS diode upon a silicon wafer obtained by the production method of the present invention for evaluation of oxide layer breakdown voltage. A silicon oxide layer 2 is formed upon a silicon wafer 1. Upon the silicon wafer 1 then is formed a two-layer gate electrode 5 of 5 mm diameter comprising an aluminum 1 upper layer and a lower layer formed from doped polysilicon 4.

[0013] Means for evaluation of oxide layer breakdown voltage of the silicon single crystal obtained by the production method of the present invention will next be explained using Table 1.

Table 1 shows the MOS diode manufacturing steps for production in order to measure oxide layer breakdown voltage.

[0014]
[Table 1]

No.	Step	Conditions
1	wafer wash	60 seconds immersion in 1.5 wt% HF, followed by ultrapure water rinse
2	gate oxidation	high temperature oxidation at 1000°C in dry oxygen to form about 250 Å thick oxide layer
3	polysilicon layer deposition	640°C deposition temperature, non-doped polysilicon layer, 5000 Å thick
4	pre-oxidation wash	5 minutes immersion at 100°C in 97% H_2SO_4 and H_2O_2 (3:1 volume ratio), followed by rinse in ultrapure water, followed by immersion for 60 seconds in 1.5 wt% HF, followed by rinse in ultrapure water
5	polysilicon oxidation	high temperature oxidation at 900°C in dry oxygen to form about 300 Å thick oxide layer
6	ion implantation	n-type : P doped at 5×10^{15} cm^{-2}, acceleration voltage of 30 keV; p-type : B doped at 10^{16} cm^{-2}, acceleration voltage of 80 keV
7	pre-anneal wash	5 minutes immersion at 100°C in 97% H_2SO_4 and H_2O_2 (3:1 volume ratio), followed by rinse in ultrapure water, followed by immersion for 60 seconds in 1.5 wt% HF, followed by rinse in ultrapure water
8	drive-in anneal	30 minutes in nitrogen at 900°C
9	polysilicon layer etching	in mixture of 40% NH_4F : 50% HF at 10 : 1 volume ratio
10	Al evaporation-attachment	resistance heating evaporation-attachment, 2000 - 5000 Å
11	lithography	positive resist, 1 μm thick
12	Al etching	in mixture of 85% H_3PO_4 : 70% HNO_3 at 19 : 1 volume ratio
13	polysilicon etching	reactive plasma etching, CF_4
14	resist removal	C washing (J100 at 100°C for 10 minutes × 2, in trichloroethylene at 86°C for 5 minutes × 2, in trichloroethylene at 86°C for 10 minutes × 1, followed by infrared drying)
15	hydrogen anneal	in H_2 (2×10^3 cc/minute) + N_2 (10×10^3 cc/minute) at 400°C for 30 minutes
16	resist application	2 μm resist thickness
17	backside polysilicon etching	reactive plasma etching, CF_4
18	resist application	2 μm resist thickness
19	backside polysilicon oxide layer etching	in mixture of 40% NH_4F : 50% HF at 10 : 1 volume ratio
20	backside electrode evaporation-attachment	electron bombardment heating, about 2000 Å thickness, p-type = Au, n-type = AuSb
21	resist removal	C washing (J100 at 100°C for 10 minutes × 2, in trichloroethylene at 86°C for 5 minutes × 2, in trichloroethylene at 86°C for 10 minutes × 1, followed by infrared drying)
22	measurement of oxide layer breakdown voltage	voltage ramping method

[0015] The CZ silicon ingot first undergoes typical silicon wafer processing comprising slicing, lapping, polishing, etc. to obtain a wafer. Thereafter the wafer undergoes a four-step additional heat treatment

comprising: 110 minutes at 1000°C in a steam atmosphere, 420 minutes at 1200°C in a nitrogen atmosphere, 70 minutes at 900°C in a dry oxygen atmosphere, and 130 minutes at 1000°C in a steam atmosphere, followed by removal of the thermal oxide layer of the silicon by dilute hydrofluoric acid solution. The obtained wafer is then washed (1), and gate oxidation is carried out to form a SiO_2 layer (2). A polysilicon layer is deposited (3). Then this polysilicon is doped by ion implantation (6). Oxidation pre-washing (4) and polysilicon oxidation (5) are pre-treatments prior to ion implantation (6). Then pre-anneal washing is performed (7). Drive-in annealing is used to fix dopant within the polysilicon (8). The polysilicon oxide layer is removed by etching (9). An aluminum layer is formed by vaporization-attachment of aluminum (10). Thereafter a positive resist film is applied and patterned during lithography (11) in order to form two-layer gate electrodes of 5 mm diameter. Thereafter the aluminum layer is etched (12), the polysilicon layer is etched (13), and then the resist layer is removed (14). Finally after hydrogen annealing to stabilize the Si-silicon oxide interface (15), a resist layer is applied to the surface to protect the MOS diodes (16), and plasma etching is used to remove the backside polysilicon layer (17). A protective resist layer is again applied to the surface (18), and the backside oxide layer is removed by etching (19). A backside electrode is formed by evaporation-attachment of gold (in the case of p-type) or gold-antimony alloy (in the case of n-type) (20). Finally, after removal of the protective resist layer (21), a voltage ramping method is used to evaluate oxide layer breakdown voltage characteristics (22). The voltage ramping method is taken to mean a method for the step-wise application of DC voltage over time as an applied current flows between aluminum layer 3 and the backside electrode of Figure 1 to inject numerous carriers from the substrate. For the present invention, the per-step voltage increase of this voltage ramping method was 0.25 MV/cm, and the holding time period was 200 ms/step.

[0016] Moreover, in carrying out the present invention, a four-step heat treatment was added comprising: 110 minutes at 1000°C in a steam atmosphere, 420 minutes at 1200°C in a nitrogen atmosphere, 70 minutes at 900°C in a dry oxygen atmosphere, and 130 minutes at 1000°C in a steam atmosphere, followed by removal of the thermal oxide layer on the silicon by dilute hydrofluoric acid solution. This additional treatment is nearly that undergone during actual device processing.

[0017] As a result of detailed investigation of the formation of oxygen precipitates under various types of crystal cooling conditions, the inventors of the present invention discovered the following relationship between cooling conditions and formation of oxygen precipitates. Point defects present in thermal equilibrium in the vicinity of the solid-melt interface are taken up by the crystal during solidification and then become supersaturated as the crystal cools. Due to diffusion of the supersaturated point defects, outward diffusion and gradient-driven diffusion toward the solid-melt interface occur so that concentration drops. Supersaturation of point defects increases due rapid cooling of the crystal. As cooling progresses, supersaturation of point defects exceeds a critical value in the vicinity of 1080°C, and point defects begin to agglomerate with one another. These agglomerates become nuclei for oxygen precipitates. However, at the high temperature side just prior to initiation of agglomeration of supersaturated point defects, concentration drops due to disappearance of point defects. This

concentration drop lowers the temperature of initiation of agglomeration between point defects (i.e., lowers the temperature of initiation of formation of oxygen precipitates), suppresses growth of oxygen precipitates, and decreases the size of oxygen precipitates. Due to these mechanisms, a crystal that is gradually cooled at a temperature of 850°C to 1080°C, which is below the temperature of initiation of agglomeration of point defects, has a marked lowering of oxygen precipitates in comparison to a crystal in which point defect agglomeration proceeds without such cooling. Moreover, a crystal that has undergone gradual cooling at 1080°C to 1200°C, which is the temperature immediately prior to initiation of agglomeration of point defects, has oxygen precipitates of markedly small size in comparison to a crystal that hasn't undergone such gradual cooling.

[0018] However, when device heat treatment is added, small sized oxygen precipitates are readily eliminated by 1st stage heat treatment at 1000°C. In contrast, large sized oxygen precipitates grow rather than disappear during 1st stage heat treatment. All oxygen precipitates formed during crystal production grow markedly independent of the size of the oxygen precipitate. Defects that cause A mode failure of oxygen layer breakdown voltage after device heat treatment are not eliminated by 1st stage heat treatment, and these defects cause oxygen precipitates which grow. The post-device-heat-treatment oxide layer breakdown voltage A mode rate is determined by the density of oxygen precipitates remaining after 1st stage heat treatment. Therefore post-device-heat-treatment oxide layer breakdown voltage improves due to lowering of oxygen precipitate density of a crystal that has undergone gradual cooling over 850°C to 1080°C during crystal production. A crystal that has undergone 1080°C to 1200°C heat treatment has an improved post-device-heat-treatment oxide layer breakdown voltage due to lowering of the size of oxygen precipitates. The inventors of the present invention, with respect to a method for gradual cooling during a certain crystal temperature region during manufacture of silicon single crystal, discovered that post-device-heat-treatment oxide layer breakdown voltage was improved when the temperature of slowest cooling was within the temperature range of 850°C to 1200°C. It was also found that oxide layer breakdown voltage was improved when the rate of cooling was 1.0°C/minute or less in the temperature region of T ± 100°C.

[0019]

[Working Examples] Although working examples of the present invention are presented below, of course the present invention isn't limited by these working examples.

[0020] Working Example 1

No particular limitation is placed upon the single crystal production apparatus used for the present invention as long as this is used for silicon single crystal production by the conventional CZ method. A production apparatus such as that shown in Figure 2 was used for the present working example.

[0021] This CZ method type silicon single crystal production apparatus is a crystal pulling furnace 21 that contains a growing silicon single crystal ingot S and a crucible 26 comprising a quartz crucible 26a

and a graphite crucible 26b which protects quartz crucible 26a. Quartz crucible 26a holds silicon melt M. At the lateral surface of crucible 26 are placed a heater 24 and a thermal insulator 23 surrounding heater 24 for prevention of the escape of heat to the exterior of the crystal pulling furnace. This crucible 26 is connected to a non-illustrated drive and a rotation shaft 25. This crucible 26 is rotated at a certain rate by this drive while crucible 26 is raised and lowered in order to prevent lowering of the silicon melt surface in accompaniment with decrease of the silicon melt within crucible 26. A pull cable 27 is provided hanging vertically down within pulling furnace 21. A chuck 29 for holding a seed crystal 28 is provided at the bottom tip of this cable 27. This pull cable 27 is wound up by a cable winding mechanism 22 so that the silicon single crystal ingot is pulled up. Ar gas is fed from gas feed port 30 formed within this pulling furnace 21. This gas flows throughout the interior of pulling furnace 21 and discharges through gas flow port 31. This type of discharge of Ar gas prevents mixing into the silicon melt of SiO generated within pulling furnace 21 by melting of silicon. A temperature control device 40 is provided for gradual cooling of the crystal within pulling furnace 21. An insulation member or heater, etc. placed surrounding the produced silicon single crystal may be used with advantage as temperature control device 40.

[0022] This apparatus was used during production of silicon single crystals under multiple conditions described below. Each of these crystals was cooled at a minimum cooling rate within the temperature region of 850°C to 1200°C, and each crystal was always cooled at 1.0°C/minute or less in the T ± 100°C temperature region.

[0023] Table 2 shows production conditions, etc. for multiple silicon single crystals grown under these conditions.

[0024]
[Table 2]

Crystal	Minimum cooling rate temperature (°C)	Conductivity type (dopant)	Crystal diameter (inches)	Resistivity (Ω cm)	Oxygen concentration * (10^{17} cm^{-3})	Carbon concentration * (10^{17} cm^{-3})
A	860	p (P)	6	2.0	10.0 - 10.5	< 1.0
B	950	n (B)	8	10.0	9.5 - 10.0	< 1.0
C	1080	p (B)	6	2.0	8.0 - 9.0	< 1.0
D	1190	n (P)	8	4.0	7.5 - 8.5	< 1.0

* These were calculated using coefficients according to the Japan Electronics Industry Development Association.

[0025] Post-device-heat-treatment oxide layer breakdown voltage of wafers sliced from these ingots was determined as shown in Figure 3. The fraction of MOS diodes showing a mean electrical field of 4.0 MV/cm or less when current density through the oxide layer of the silicon wafer was 1 $\mu A/cm^2$ relative to the total number of MOS diodes (A mode fraction) in each case was less than 3%. This

indicates that wafers sliced from silicon single crystal ingot produced by the method of the present invention have good oxide layer breakdown voltage characteristics.

[0026] Working Example 2

The apparatus of working example 1 was used during production of multiple silicon single crystals under conditions listed below. Each of these crystals was cooled at a minimum cooling rate within the temperature region of 850°C to 1200°C, and each crystal was always cooled at 1.0°C/minute or less in the T ± 100°C temperature region.

[0027] Table 3 shows production conditions, etc. for multiple silicon single crystals grown under these conditions.

[0028]

[Table 3]

Crystal	Minimum cooling rate temperature (°C)	Conductivity type (dopant)	Crystal diameter (inches)	Resistivity (Ω cm)	Oxygen concentration * (10^{17} cm^{-3})	Carbon concentration * (10^{17} cm^{-3})
E	860	n (P)	8	4.0	8.0 - 9.0	< 1.0
F	950	p (B)	6	2.0	10.0 - 10.5	< 1.0
G	1080	p (B)	6	10.0	8.0 - 9.0	< 1.0
H	1190	n (P)	8	4.0	7.5 - 8.5	< 1.0

* These were calculated using coefficients according to the Japan Electronics Industry Development Association.

[0029] Post-device-heat-treatment oxide layer breakdown voltage of wafers sliced from these ingots was determined as shown in Figure 3. The fraction of MOS diodes showing a mean electrical field of 4.0 MV/cm or less when current density through the oxide layer of the silicon wafer was 1 $\mu A/cm^2$ relative to the total number of MOS diodes (A mode fraction) in each case was less than 3%. This indicates that wafers sliced from silicon single crystal ingot produced by the method of the present invention have good oxide layer breakdown voltage characteristics.

[0030] Comparative Example 1

The apparatus of working example 1 was used during production of multiple silicon single crystals under conditions listed below. Each of these crystals was cooled such that minimum cooling rate wasn't within the temperature region of 850°C to 1200°C, and each crystal wasn't cooled at 1.0°C/minute or less in the T ± 100°C temperature region.

[0031] Table 4 shows production conditions, etc. for multiple silicon single crystals grown under these conditions.

[0032]
[Table 4]

Crystal	Minimum cooling rate temperature (°C)	Conductivity type (dopant)	Crystal diameter (inches)	Resistivity (Ω cm)	Oxygen concentration * (10^{17} cm^{-3})	Carbon concentration * (10^{17} cm^{-3})
TA	840	n (P)	6	2.0	10.0 - 10.5	< 1.0
TB	1220	p (B)	8	10.0	9.5 - 10.0	< 1.0
TC	no slow cooling	p (B)	6	2.0	8.0 - 9.0	< 1.0
TD	no slow cooling	n (P)	8	4.0	7.5 - 8.5	< 1.0

* These were calculated using coefficients according to the Japan Electronics Industry Development Association.

[0033] Post-device-heat-treatment oxide layer breakdown voltage of wafers sliced from these ingots was determined as shown in Figure 5. The fraction of MOS diodes showing a mean electrical field of 4.0 MV/cm or less when current density through the oxide layer of the silicon wafer was 1 $\mu A/cm^2$ relative to the total number of MOS diodes (A mode fraction) in each case was at least 3% which indicates oxide layer breakdown voltage characteristic wasn't good.

[0034] Comparative Example 2

The apparatus of working example 1 was used during production of multiple silicon single crystals under conditions listed below. Each of these crystals was cooled such that minimum cooling rate wasn't within the temperature region of 850°C to 1200°C, and each crystal was cooled at a rate of 1.0°C/minute or less in the T ± 100°C temperature region.

[0035] Table 5 shows production conditions, etc. for multiple silicon single crystals grown under these conditions.

[0036]
[Table 5]

Crystal	Minimum cooling rate temperature (°C)	Conductivity type (dopant)	Crystal diameter (inches)	Resistivity (Ω cm)	Oxygen concentration * (10^{17} cm^{-3})	Carbon concentration * (10^{17} cm^{-3})
TE	800	p (B)	8	4.0	8.0 - 9.0	< 1.0
TF	840	n (P)	6	2.0	10.0 - 10.5	< 1.0
TG	1220	p (B)	6	10.0	8.0 - 9.0	< 1.0
TH	1300	n (P)	8	4.0	7.5 - 8.5	< 1.0

* These were calculated using coefficients according to the Japan Electronics Industry Development Association.

[0037] Post-device-heat-treatment oxide layer breakdown voltage of wafers sliced from these ingots was determined as shown in Figure 6. The fraction of MOS diodes showing a mean electrical field of 4.0 MV/cm or less when current density through the oxide layer of the silicon wafer was 1 $\mu A/cm^2$

relative to the total number of MOS diodes (A mode fraction) in each case was at least 3% which indicates oxide layer breakdown voltage characteristic wasn't good.

[0038]

[Results of the Invention] Silicon single crystal of the present invention and silicon single crystal produced by the method of the present invention, due to excellent device characteristics (particularly post-device-heat-treatment oxide layer breakdown voltage characteristics), is appropriate for wafers for MOS devices and devices that have various types of structures.

[Simple Explanation of the Figures]

[Figure 1] This is a partial cross-sectional drawing of a MOS diode formed upon a silicon wafer for evaluation by the conventional method for determination of oxide layer breakdown voltage characteristics of silicon single crystal.

[Figure 2] This is a schematic drawing showing the CZ method type silicon single crystal production apparatus used in the working examples of the present invention.

[Figure 3] This shows post-device-heat-treatment oxide layer breakdown voltage of multiple crystals of working example 1 of the present invention.

[Figure 4] This shows post-device-heat-treatment oxide layer breakdown voltage of multiple crystals of working example 2 of the present invention.

[Figure 5] This shows post-device-heat-treatment oxide layer breakdown voltage of multiple crystals of comparative example 1.

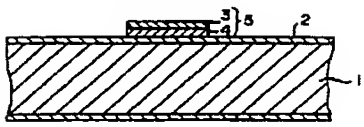
[Figure 6] This shows post-device-heat-treatment oxide layer breakdown voltage of multiple crystals of comparative example 2.

[Explanation of Items]

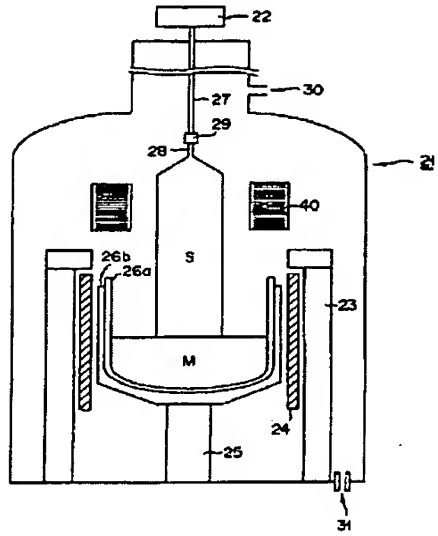
1	....	silicon wafer
2	....	silicon oxide layer (insulation oxide layer)
3	....	aluminum layer
4	....	polysilicon layer
5	....	two-layer gate electrode
21	....	crystal pulling furnace (CZ method silicon single crystal production apparatus)
22	....	cable winding mechanism
23	....	thermal insulator
24	....	crucible
26a	....	quartz crucible
26b	....	graphite crucible
27	....	pull cable
28	....	seed crystal
29	....	chuck
30	....	gas feed port

31	....	gas discharge port
40	....	temperature control device (crystal annealing device)
M	....	silicon melt
S	....	silicon single crystal ingot

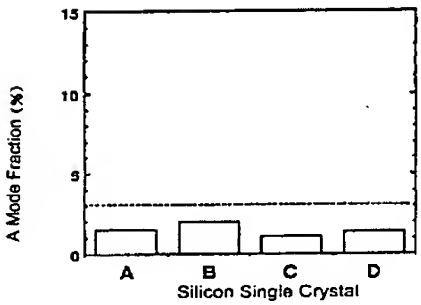
[Figure 1]



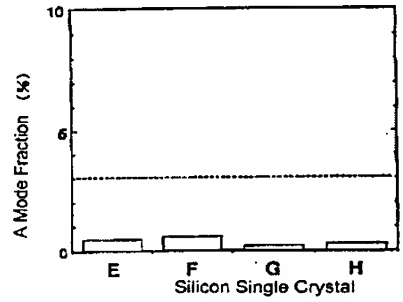
[Figure 2]



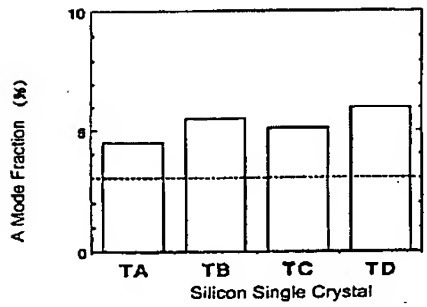
[Figure 3]



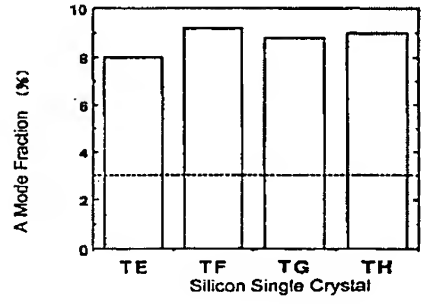
[Figure 4]



[Figure 5]

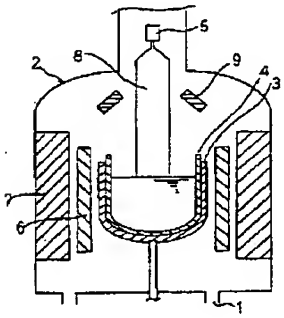


[Figure 6]

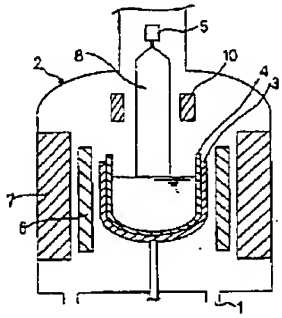


12 .... thermal insulator
13 .... radiation shield

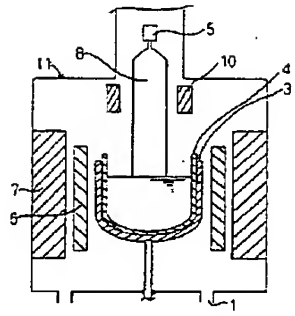
[Figure 1]



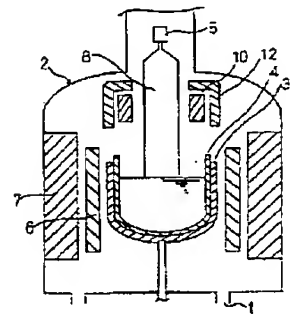
[Figure 2]



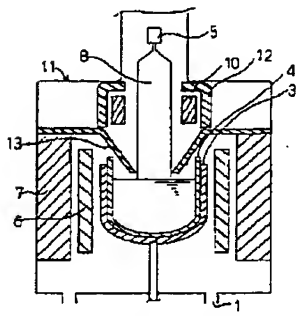
[Figure 3]



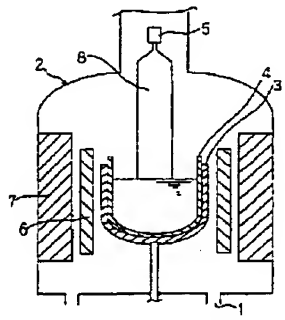
[Figure 4]



[Figure 5]



[Figure 6]



[Figure 7]